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| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.         | CONFIRMATION NO.       |
|--|-------------|----------------------|-----------------------------|------------------------|
| 10/721,524   | 11/25/2003  | Richard A. Blanchard | 03-C-040 (850063.602)       | 5333                   |
| 30423 7590 08/31/2007<br>STMICROELECTRONICS, INC.<br>MAIL STATION 2346<br>1310 ELECTRONICS DRIVE<br>CARROLLTON, TX 75006 |             |                      | EXAMINER<br>DICKY, THOMAS L |                        |
|  |             |                      | ART UNIT<br>2826            | PAPER NUMBER           |
|  |             |                      | MAIL DATE<br>08/31/2007     | DELIVERY MODE<br>PAPER |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

|                              |                                      |   |  |
|------------------------------|--------------------------------------|---|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>10/721,524 | <b>Applicant(s)</b><br>BLANCHARD ET AL. |  |
|                              | <b>Examiner</b><br>Thomas L. Dickey  | <b>Art Unit</b><br>2826                 |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 20 February 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☐ Claim(s) 13-27, 34-47 and 50-52 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13-27 and 34-46 is/are allowed.
- 6) ☒ Claim(s) 47 and 50-52 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>02/20/2007</u> . | 6) <input type="checkbox"/> Other: _____  |

Art Unit: 2826

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments, see page 2 of the remarks filed 2/20/07, with respect to the rejection(s) of claim(s) 47 and 50-52 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However upon further consideration, a new ground(s) of rejection is made.

### ***Information Disclosure Statement***

2. The Information Disclosure Statement filed on 02/20/2007 has been considered.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 47 and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over CHAN ET AL. (5,917,226) in view of Shaw et al. (5,847,454).

With regard to claim 47 Chan et al. discloses a beam structure comprising a semiconductor substrate 21'; a first conducting layer 23', a beam 20 positioned relative to the

Art Unit: 2826

substrate 21', the beam 20 being connected at a first portion 24' thereof to the substrate 21'; the beam 20 being movable at a second portion 26'; a remaining sacrificial layer 25' (the right of the two layers marked 25') between the first portion 24' of the beam 20 and the substrate 21'; and a circuit 12 configured to detect electrical contact between the second portion 26' of the beam 20 and the first conducting layer. Note figures 1,3,5, and column 6 lines 14-67 of Chan et al. Chan et al. does not disclose that positioning beam 20 within a trench having walls extending into the semiconductor substrate 21', positioning first conducting layer 23' over the walls of the trench at selected locations and spacing second portion 26' from the walls of the trench by a selected distance.

However, Shaw et al. discloses a method of forming a beam structure comprising positioning beam 52 within a trench 54 having walls 78 extending into semiconductor substrate 50, positioning a first conducting layer 78 (same # but different part from the walls) over the walls 78 of trench 54 at selected locations and spacing a second portion 74 from the walls of the trench 54 by a selected distance. Note figures 1A-1J, 3, column 13 lines 36-48, and column 14 lines 1-41 of Shaw et al. It would have been obvious to a person having skill in the art to modify Chan et al.'s beam structure by using the trenching method taught by Shaw et al. to position Chan et al.'s beam 20 within a trench having walls extending into semiconductor substrate 21', positioning first conducting layer 23' over the walls of the trench at selected locations and spacing a second portion 26' from the walls of the trench by a selected distance, thus achieving the claimed inven-

Art Unit: 2826

tion. It is noted that Shaw et al. teaches, "The process of the present invention permits fabrication of integrated structures, wherein released beams and other microelectromechanical structures may be interconnected with an on-chip integrated circuit (IC). In accordance with this modification of the process, which is illustrated in FIGS. 5A-5I, an integrated circuit 12 wafer can be batch fabricated using standard integrated circuit technologies to produce desired circuits and circuit components on the wafer, and thereafter a microelectromechanical device can be fabricated on the wafer utilizing the process of the present invention without varying the standard IC technology" (column 14 lines 46-54); and that "Any kind of integrated circuit can be on the wafer for connection to the released structure" (column 15 lines 31-34). From these statements it is possible to infer that application of Shaw et al.'s trenching technique can be applied to modify Chan et al.'s combination of beam 20 and circuit 12 with a reasonable expectation of successfully producing the claimed device. The Examiner explicitly states that the reason (See *KSR International Co. v. Teleflex Inc.*, 550 U. S. \_\_\_ (2007), slip op. at 14) the combination would have been obvious is that the claimed combination is nothing more than the application of a known technique (the trenching method of Shaw et al.) to a piece of prior art (Chan et al.'s) ready for improvement, with a reasonable expectation of success.

In a case such as this one, "where an improvement is no more than 'the simple substitution of one known element for another or the mere application of a known technique

Art Unit: 2826

to a piece of prior art ready for improvement,' *KSR Int'l Co. v. Teleflex Inc.*, [127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)], no further analysis is required of the Examiner." *Ex parte Smith*, 83 USPQ2d 1509, 1518 (Bd. Pat. App. & Int. 2007) (Or see Slip Op., available at <http://www.uspto.gov/web/offices/dcom/bpai/prec/fd071925.pdf>, at 21).

With regard to claims 50-52 Chan et al. discloses a beam structure comprising a semiconductor substrate 21'; a beam 20 positioned relative to the substrate 21', coupled to the substrate 21' at a first portion 24' and a third portion 25' (on the left, opposite part 24') thereof and movable with respect to the substrate 21' at a second portion 26' thereof located between the first 24' and third 25' portions; and means comprising an electrical circuit 12 having a first input coupled to the beam 20 and a second input coupled to the substrate 21', the electrical circuit 12 configured to detect electrical continuity between the first and second inputs, for detecting contact between the second portion 26' of the beam 20 and the substrate 21'. Note figures 1,3,5, and column 6 lines 14-67 of Chan et al. Chan et al. does not disclose positioning beam 20 within a trench extending in semiconductor substrate 21', or making the contact between the second portion 26' of the beam 20 and the substrate 21' at a wall of the trench.

However, Shaw et al. discloses a method of forming a beam structure comprising positioning beam 52 within a trench 54 extending in semiconductor substrate 50, and making contact between a second portion 26' of the beam 52 and the substrate 50 at a

Art Unit: 2826

wall 78 of the trench 54. Note figures 1A-1J, 3, column 13 lines 36-48, and column 14 lines 1-41 of Shaw et al. It would have been obvious to a person having skill in the art to modify Chan et al.'s beam structure by using the trenching method taught by Shaw et al. to position beam 20 within a trench extending in semiconductor substrate 21', and making contact between second portion 26' of beam 20 and the substrate 50 at a wall of the trench, thus achieving the claimed invention. It is noted that Shaw et al. teaches, "The process of the present invention permits fabrication of integrated structures, wherein released beam 20s and other microelectromechanical structures may be interconnected with an on-chip integrated circuit 12 (IC). In accordance with this modification of the process, which is illustrated in FIGS. 5A-5I, an integrated circuit 12 wafer can be batch fabricated using standard integrated circuit 12 technologies to produce desired circuit 12s and circuit 12 components on the wafer, and thereafter a microelectromechanical device can be fabricated on the wafer utilizing the process of the present invention without varying the standard IC technology" (column 14 lines 46-54); and that "Any kind of integrated circuit 12 can be on the wafer for connection to the released structure" (column 15 lines 31-34). From these statements it is possible to infer that application of Shaw et al.'s trenching technique can be applied to modify Chan et al.'s combination of beam 20 and circuit 12 with a reasonable expectation of successfully producing the claimed device. The Examiner explicitly states that the reason (See *KSR International Co. v. Teleflex Inc.*, 550 U. S. \_\_ (2007), slip op. at 14) the combination

Art Unit: 2826

would have been obvious is that the claimed combination is nothing more than the application of a known technique (the trenching method of Shaw et al.) to a piece of prior art (Chan et al.'s) ready for improvement, with a reasonable expectation of success.

In a case such as this one, "where an improvement is no more than 'the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement,' *KSR Int'l Co. v. Teleflex Inc.*, [127 S.Ct. 1727, 1740, 82 USPQ2d 1385, 1396 (2007)], no further analysis is required of the Examiner." *Ex parte Smith*, 83 USPQ2d 1509, 1518 (Bd. Pat. App. & Int. 2007) (Or see Slip Op., available at <http://www.uspto.gov/web/offices/dcom/bpai/prec/fd071925.pdf>, at 21).

#### ***Allowable Subject Matter***

4. Claim 13-27 and 34-46 are allowed over the references of record for the reasons recited in the action mailed 11/17/2006.

#### ***Conclusion***

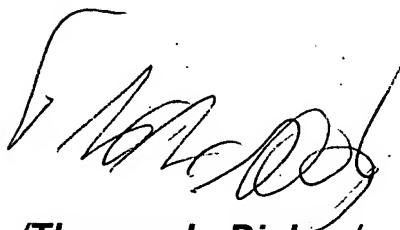
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the



Art Unit: 2826

organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'T. L. Dickey', is written over a horizontal line.

**/Thomas L. Dickey/  
Primary Examiner  
Art Unit 2826**